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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of: James Digby Collier et al.
Title: INTEGRATED CIRCUIT
Attorney Docket No.: 491.039US1

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- X Specification (20 pgs, including claims numbered 1 through 30).
- X Formal Drawing(s) (7 sheets).
- X Unsigned Combined Declaration and Power of Attorney (3 pgs).

X Information Disclosure Statement (1 pgs), Form 1449 (1 pgs), and copies of cited references (7).
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INTEGRATED CIRCUIT

The present invention relates to a semiconductor integrated circuit and more particularly to a CMOS or similar type of circuit when used in a frequency divider circuit ("pre-scaler").

In many high frequency radio receivers a synthesiser and a voltage controlled oscillator are required to generate the local carrier signal that is used to perform a first demodulation of the received high frequency radio signal. However, the synthesiser is generally unable to take the high frequency carrier signal directly as an input. Therefore a pre-scaler must be used to divide the carrier frequency down to a frequency that can be accepted by the synthesiser. A pre-scaler circuit generally comprises a number of divide by 2 circuits and some control logic to provide, for example, a divide by 16 or 17 circuit. Each divide by 2 circuit generally comprises a pair of latch circuits connected in a master slave configuration.

In a conventional CMOS latch circuit capable of lower frequency operation, a signal on the data input is passed through to the output while the clock signal is high. When the clock signal goes low the latch maintains the same output until the clock signal goes high again, when a new data value is allowed through. The conventional CMOS latch comprises two inverters connected in series and two transmission gates. The data input of the latch is connected to the input of the first inverter through one of the transmission gates. The output of the second inverter (which is also the output of the latch) is fed back to the input of the first inverter through the other transmission gate. To prevent the feedback and the data input interfering with each

other, the two transmission gates are driven by antiphase clock signals such that when one is open the other is closed.

The maximum frequency at which the latch can be clocked depends on the speed at which the transmission gates can open and close, and of course the propagation delay through the inverters. The CMOS transmission gates require to be driven with clock signals having substantially the full swing of the power supply voltage between states. The maximum operating frequency of a CMOS latch is therefore in practice much lower than that of a latch constructed in a suitable high frequency bipolar technology such as ECL. Furthermore, CMOS circuits consume a lot of power at high frequencies, therefore, when high speed pre-scalers are required bipolar technology is invariably used, whereas for low speed digital devices CMOS or other MOS technology is often preferred. In applications where both high speed and low speed digital functions are required, it is therefore commonly necessary to employ two separate chips, one using CMOS technology for performing the low speed digital functions and the other using bipolar technology for performing high speed digital and analogue functions. The need for two separate chips increases the cost and size of the final product. Alternatively, a more complex and expensive IC process which supports both bipolar and CMOS transistors could be used.

According to one aspect, the present invention provides a frequency divider circuit comprising a number of amplifier stages connected in series with the output of a terminating amplifier stage connected to the input of a preliminary amplifier stage and modulating means responsive to an input signal to be frequency divided, for modulating the propagation delay through each of the amplifier stages such that when the propagation delay

through one set of amplifier stages increases, the propagation delay through the other amplifier stages decreases.

The present invention also provides a semiconductor latch comprising: a data input, a data output, a clock input, two inverters connected in a memory arrangement with the output of one connected to the input of the other and input means connected to the memory arrangement for writing new data applied to the data input into said memory arrangement, independence upon a clock signal applied to said clock input, characterised in that the latch comprises varying means for varying the time taken for new data to be written into said memory arrangement.

The present invention also provides a method of frequency division using a number of amplifier stages connected in series with the output of the last amplifier stage connected to the input of the first amplifier stage, the method comprising: modulating the propagation delay through each of the amplifier stages such that when the propagation delay through a given group of amplifiers stages increases, the propagation through another group of amplifier stages decreases.

The frequency divider or latch circuit embodying the present invention can be used in many applications. For example, it can be used to generate a local carrier in a radio receiver circuit.

Embodiments of the invention will now be described, by way of example only, with reference to the accompanying drawings in which:

Figure 1a shows a latch circuit according to a first embodiment of the present invention;

Figure 1b shows a logic equivalent circuit of the latch circuit shown in Figure 1a;

Figure 2 shows two of the latches shown in Figure

1a cascaded together and connected to form a divide by 2 frequency divider;

Figure 3 is a generalised equivalent circuit of the frequency divider shown in Figure 2, with each latch being represented by a differential amplifier with hysteresis and a modulation block;

Figure 4 shows a frequency divider circuit according to a second embodiment of the present invention;

Figure 5 schematically shows the input/output relationship of the differential amplifiers with hysteresis used in the second embodiment;

Figure 6 shows a second embodiment of a latch circuit that may be employed in the frequency divider circuit shown in Figure 4;

Figure 7a is a circuit diagram that demonstrates how the latch circuit shown in Figure 1a can be modified to provide additional logic functions;

Figure 7b shows a logic equivalent circuit of the latch circuit shown in Figure 7a;

Figure 8 is a circuit diagram showing a divide by four/five circuit using latch circuits according to embodiments of the present invention;

Figure 9 shows a simplex frequency modulated radio transmitter and receiver for digital data of relatively low bit rate, according to an embodiment of the present invention.

Figure 1a shows a latch circuit generally indicated by reference numeral 10, according to an embodiment of the present invention and Figure 1b shows a logic equivalent circuit thereof. The latch has clock inputs CLK, a data input D, a complementary data input DB, a data output Q and a complementary data output QB. In the present description and drawings, the suffix "B" is used throughout to indicate the complement of a given logic

signal such that when Q = 0, QB = 1 and vice versa.

In the circuit of Figure 1a, p-channel MOS transistor P1 and n-channel MOS transistor N1 form a first CMOS inverter 1 with input Q and output QB and p-channel transistor P2 and n-channel transistor N2 form a second inverter 3 with input QB and output Q. The two inverters 1 and 3 are connected in an arrangement similar to a standard static memory cell, with the output of one connected to the input of the other, as shown in Figure 1b. This is in contrast to the more typical CMOS latch using transmission gates, described above. The circuit also comprises two pairs of n-channel transistors connected in series (N3 and N5; N4 and N6) each of which performs a NAND type function having inputs D and CLK, and DB and CLK respectively, and outputs QB and Q respectively. These two NAND type circuits are represented by NAND gates 5 and 7 in the logic equivalent circuit shown in Figure 1b, and will be referred to hereinafter as NAND gates 5 and 7. However, as those skilled in the art will appreciate, these circuits do not form complete CMOS NAND gates.

In operation, provided CLK remains low, the positive feedback connection between inverters 1 and 3 maintains the latch in whatever is its present state (Q low/QB high) or Q high/QB low). When CLK goes high, however, the state of the latch can be changed, depending on the data inputs D/DB. For example, if a logic high is on QB and a logic high is applied to CLK while D is high, then QB is forced to a logic low. Similarly, if a logic high is on Q and a logic high is applied to CLK while DB is high, then Q is forced to a logic low. When CLK goes low again, the new state is preserved.

The n-channel transistors N1 and N2 of the two inverters 1 and 3 are made "weaker" than the transistors in the corresponding NAND gate 7 and 5 that drives them,

so that the logic level within the memory cell arrangement can be overwritten. This is achieved in the present embodiment by reducing the width to length ratio (aspect ratio) of the transistors N1 and N2 compared to the aspect ratio of transistors N3, N5 and N4, N6. Table 1 below lists suitable dimensions for each of the transistors shown in Figure 1A, in 0.7 μm and 0.5 μm processes as alternatives. The transistors N3, N4 responsive to the clock signal CLK are made particularly "strong".

Table 1

Transistor	Width : Length (0.7 μm Process)	Width : Length (0.5 μm Process)
P1	6 : 1	8 : 0.5
P2	6 : 1	8 : 0.5
N1	2.2 : 0.7	2.2 : 0.5
N2	2.2 : 0.7	2.2 : 0.5
N3	32 : 0.7	32 : 0.5
N4	32 : 0.7	32 : 0.5
N5	6 : 0.7	8 : 0.5
N6	6 : 0.7	8 : 0.5

The propagation delay through the latch 10 is dependent upon the time taken to force either Q or QB into a logic low after D/DB changes. If an analogue signal is applied to CLK instead of a logic signal, transistors N3 and N4 are not necessarily fully open or fully closed, but act as variable resistances, the values of which fluctuate in response to the clock signal (CLK). As a result of this fluctuating resistance, the time

taken to force the latch 10 into each different state is modulated and so the propagation delay through the latch 10 is modulated.

The inventors have found that by utilising the delay modulation effect of this type of latch, a pre-scaler circuit can be made which is capable of operating at much higher frequencies than those currently available in current CMOS technology. In particular, by applying an oscillating signal to the CLK input, the propagation delay can be modulated successfully even at a frequency which is far too high for normal "digital" operation of the latch.

Figure 2 shows two such latch circuits 10a and 10b connected together to form a divide by 2 frequency divider. The Q and QB outputs of the first latch 10a are connected to the D and DB inputs respectively of the second latch 10b, and the Q and QB outputs of the second latch 10b are connected to the DB and D inputs respectively of the first latch 10a. The input signal (IN) whose frequency is to be divided is applied to the clock input CLK of the first latch 10a, and an antiphase version (INB) of the input signal to be divided is applied to the clock input CLK of the second latch 10b. The signals IN and INB oscillate with a certain amplitude about a voltage midway between logic high and low levels.

Connected in this manner, the circuit acts as a ring oscillator and a chain of logic high and logic lows propagate round. The rate at which the logic high and logic lows propagate depends upon the propagation delay through each latch 10a and 10b. If the delay through latch 10a is T_1 and the delay through latch 10b is T_2 then the oscillation frequency = $1/(T_1 + T_2)$.

If the delays T_1 and T_2 are made to vary cyclically, with frequency f_{in}, about a value of $1/f_{in}$, (i.e. $1/f_{in} < T_1$ and $T_2 < 1/f_{in}$) such that T_1 increases when T_2 decreases

and vice versa, then the logic highs and lows can only propagate round the circuit with a delay of $2/f_{in}$. Any signal that tries to propagate round the circuit any faster or slower than this will automatically be slowed down or speeded up, as the case may be, due to the alternating delay values. In this way, the circuit becomes an oscillator locked at frequency $f_{in}/2$, and thereby forms a frequency divider, since f_{in} is the frequency of the input signal IN/INB. When viewed in this way, the operation of the circuit can be likened to a so-called parametric amplifier.

The inventors have established that by performing the frequency division operation in this manner, a CMOS pre-scaler circuit can operate at frequencies (f_{in}) up to about 600 MHz, using only a conventional 0.7 μm CMOS process. The ability to operate at these frequencies permits the integration of more functions on a single chip.

To explain how the frequency divider shown in Figure 2 operates at a different level, it is useful to consider each latch 10a and 10b as being a differential amplifier with hysteresis having a modulation input that can be used to vary the propagation delay through the amplifier. In this embodiment, the modulation input amplitude modulates the inputs applied to the amplifiers, while the hysteresis remains constant.

Figure 3 is an equivalent circuit diagram of the frequency divider shown in Figure 2 with each latch 10a and 10b being represented by a differential amplifier with hysteresis 30a and 30b and a modulation block 33a and 33b as described above. Modulation block 33a is driven by the input signal (IN) to be divided and modulation block 33b is driven by the inverse (INB) of the input signal to be divided.

As mentioned above, the modulation blocks 33a and

33b act as means for varying the propagation delay of each amplifier, which is achieved in this embodiment by varying the resistance of clock transistors N3/N4 in series with input transistors N5/N6, effectively varying the strength of connection from one amplifier to the other. If the strength of the connection is reduced between amplifier 30a and amplifier 30b then it will take longer for the signal to propagate through the amplifier 30b. On the other hand, if the strength of connection is increased between amplifier 30a and amplifier 30b then it will take less time for the signal to propagate through the amplifier 30b. Similarly, the propagation delay through amplifier 30a can be varied by changing the strength of connection between amplifier 30b and amplifier 30a. In this way, delay T_1 and T_2 can be changed by varying the strength of the connection between the two amplifiers.

After generalising the circuit shown in Figure 2 to the equivalent circuit shown in Figure 3, it will be seen that the same modulation effect can be achieved in other ways, for example by modulating the hysteresis of the amplifiers directly as illustrated in Figures 4 and 5.

Figure 4 schematically shows the differential amplifiers with hysteresis connected in series and having output Q of the second amplifier 40b connected to the DB input of the first amplifier 40a, and output QB connected to the D input of the first amplifier. The input signal IN is applied to the first amplifier 40a for varying the hysteresis thereof and complementary input signal INB is applied to the second amplifier 40b for varying the hysteresis thereof.

Figure 5 schematically shows the input/output characteristic of each amplifier 40a and 40b shown in Figure 4 including hysteresis. The overall negative feedback (due to the coupling from the Q output of the

second stage to the DB input of the first) overcomes the positive feedback necessary to create hysteresis of each latch. The effect of this is such that by changing the hysteresis the effective propagation delays (T_1 and T_2) through the amplifiers change, while the strength of the connections between the amplifiers remains constant. In particular, if delays T_1 and T_2 are made to vary cyclically, with frequency f_{in} about a value of $1/f_{in}$, (i.e. $1/f_{in} < T_1$ and $T_2 > 1/f_{in}$) such that when T_1 increases T_2 decreases and vice versa then, as in the first embodiment, the logic high and lows can only propagate around a circuit with frequency $1/2f_{in}$.

Figure 6 shows a latch circuit generally indicated by reference numeral 60 which may be used to form the amplifier shown in Figure 4, namely a latch circuit whose hysteresis can be varied. The latch 60 is similar to latch 10 shown in Figure 1a, but with the transistors N3', N4' placed in series with transistors N2' and N1' respectively, rather than in series with transistors N5' and N6' respectively.

As in the first embodiment, the propagation delay through the latch 60 is dependent upon the time taken to force either Q' or QB' into a logic low. Further, when a high frequency signal is applied to CLK, transistors N3' and N4' do not necessarily have time to become fully open or fully closed, but anyhow act as variable resistances, the values of which fluctuate in response to the input signal (CLK). As a result of this fluctuating resistance, the time taken to force the latch 60 into each different state is modulated and so the propagation delay through the latch 60 is modulated. Therefore, in this embodiment the clock signal is effectively modulating the propagation delay by modulating the hysteresis of the latch circuits.

Figure 7a shows how the latch circuit shown in

Figure 1a can be modified to include other logic functions (similar modifications could be made to the latch circuit shown in Figure 6). The same reference signs are used in Figure 1a so far as possible. In particular, Figure 7a comprises a P-channel MOS transistor P1 and N-channel MOS transistor N1 which form a first CMOS inverter 1 with input Q and output QB, and P-channel transistor P2 and N-channel transistor N2 which form a second inverter 3 with input QB and output Q. As in the latch circuit shown in Figure 1a, the two inverters 1 and 3 are connected in a standard static memory cell arrangement with the output of one connected to the input of the other, as shown in Figure 7b. The latch circuit also comprises transistors N3, N6A and N6B which together form a circuit that performs a three input NAND type function having inputs A B and CLK and output QB, and is represented by NAND gates 70 and 5 in Figure 7b. The circuit also comprises transistors N6A and N6B in parallel and transistor N4 connected in series with the parallel combination of transistors N6A and N6B. The parallel combination of transistors N6A and N6B forms a circuit that performs an OR type function and is represented by OR gate 71 in Figure 7b. The transistor N4 and the above parallel combination together form a circuit that performs a NAND type function, and is represented by NAND gate 7 in Figure 7b.

The circuit shown in Figure 7a operates as follows. When QB is high and inputs A, B and CLK are all high, then QB will be forced to a logic low. Similarly, when Q is high and either (i) input AB (complement of A) and CLK are high or (ii) input (complement of B) BB and CLK are high, then Q will be forced to a logic low. In other words, the output of the latch (Q) will be low unless both inputs A and B are high when CLK is high. Therefore, the latch circuit shown in Figure 7a

effectively comprises a D-type latch whose Data input is a logical AND function of inputs A and B.

As those skilled in the art will appreciate, the addition of the extra logic circuitry will not affect the principle of operation of the latch circuit when employed in a frequency divider circuit. Therefore, the latch circuit can be employed in more complex counter circuits and still maintain the speed advantage over the known devices.

Figure 8 shows an example of a pre-scaler circuit that can perform a divide by four or divide by five operation. The circuit as shown comprises four latch circuits of the type shown in Figure 1a or Figure 6 (L2, L3, L4 and L6) and two latch circuits of the AND gate type shown in Figure 7a (L1 and L5). A control input CTRL/CTRLB is connected to the B/BB input of latch L5. The circuit will divide by four when the CTRL is low and will divide by five when the CTRL is high and can operate at frequencies up to about 450MHz from 3V supplies and up to 600 MHz at 5V, on a 0.7 μm process. The principle of operation of the circuit is the same as that of the divide by two circuit shown in Figure 2, and will not be described again.

All of the latches L1 to L5 are clocked by the input signal IN/INB whose frequency is to be divided. Alternatively, the counter circuit could comprise a plurality of divide by two circuits, like those shown in Figure 2, connected in series with the output of one divide by 2 circuit being applied to the clock input of the next adjacent divide by two circuit. This has the advantage that later stages can be dimensioned for lower speed and lower current operation, but is limited to powers of two in the choice of division factors. By providing division factors of four and five (2^7 and $2^2 + 1$) with suitable control logic, any integer division

factor greater than 4 x 5 can be achieved.

Figure 9 shows an application for the novel frequency divider circuits in the form of a simplex frequency modulated (FM) radio transmitter and receiver generally indicated by reference numeral 90, for digital data of relatively low bit rate. Applications of such a radio include mobile pagers, and also in future data transmission for control and metering of utilities such as gas and electricity supplies. The general structure of the transmitter/receiver is of a form well-known to those skilled in the art and will not be described in depth.

Referring to Figure 9, when data is to be transmitted it is first modulated in modulation block 91 using a data modulating technique such as quadrature phase shift keying (QPSK) and then supplied to the input of a voltage controlled oscillator (VCO) 93. The output of the VCO 93 is a radio frequency (RF) signal modulated by the QPSK signal which is then amplified by a power amplifier 95 and broadcast from an antenna 97 via a transmit/receive control switch 99 and filter 101.

When data is to be received, RF input signals picked up by the antenna 97 are filtered in filter 101 to remove noise and passed to an RF amplifier 103 via the transmit/receive control switch 99. The amplified signals are then filtered again in a filter 105 to remove unwanted carrier signals that might result in "image signals" at an IF stage. A mixer 107 converts the RF input signals down to intermediate frequency (IF) signals by multiplying the incoming RF signals by a locally generated carrier signal. The IF signals at the output of the mixer 107 are then filtered again by a ceramic resonator or similar filter 109 which has a flat response over the required bandwidth and large attenuation either side of the passband. The received data is then

retrieved by demodulating the IF signal output from the ceramic filter 109 in a demodulation block 111.

Although it is very effective as a filter, the centre frequency of the ceramic type filter 109 has a fixed value. It is not possible to vary this centre frequency in order to re-tune the radio to other carrier frequencies, and at the same time maintain the required attenuation on either side of the passband. The solution to this problem is to ensure that the IF signals at the output of the mixer 107 are always centred at the same frequency. Therefore, to receive other modulated carriers, the local carrier signal applied to the mixer 107 must be variable to convert the desired RF signals down to the fixed IF frequency.

This is conventionally achieved by using a voltage controlled oscillator (VCO) 93, a pre-scaler 113 and a digital frequency synthesiser 115 connected in the manner shown in Figure 5. The frequency of the output signal from the VCO 93 is controlled by the input voltage thereto supplied by the synthesiser 115, while the synthesiser receives a version of the VCO output signal, frequency divided by the pre-scaler 113.

Frequency division is conventionally thought of as a digital function and the maximum frequency the pre-scaler 113 can reduce depends on the digital circuit technology used. With RF input signals, bipolar transistor technology is normally used which can operate at the high RF frequencies. However, when a low cost, low power CMOS chip is used for the synthesiser 115 (and perhaps also for the data decoding, processing and control operations of the receiver as a whole), this results in the need for a second chip for performing the frequency division, which increases the cost and size of the transmitter/receiver 90. In contrast, the pre-scaler 103 in the transmitter/receiver of Figure 9 uses the

novel frequency divider described above. By this feature, every part of the simplex transmitter/receiver 90, with the possible exception of the analog filters, can be built into a single MOS integrated chip, thereby reducing the overall cost and size of the data transmitter/receiver 90. The mixer 107 can be implemented by MOSFET transistors also integrated on the same chip.

CLAIMS:

1. A frequency divider circuit comprising:

an even number of amplifier stages connected in series with the output of the last amplifier stage connected to the input of the first amplifier stage; and

modulating means, responsive to an input signal to be frequency divided, for modulating the propagation delay through each of said amplifier stages, about the period of the input signal to be divided, such that when the propagation delay through the odd amplifier stage(s) increases, the propagation delay through the even amplifier stage(s) decreases.

2. A frequency divider circuit according to claim 1, wherein there are two amplifier stages connected in series.

3. A frequency divider circuit comprising a plurality of frequency divider circuits according to claim 1 or 2 connected in series.

4. A frequency divider circuit according to claim 1, 2 or 3, wherein each amplifier is a differential amplifier.

5. A frequency divider circuit according to any preceding claim, wherein each amplifier stage comprises an amplifier with hysteresis.

6. A frequency divider circuit according to any preceding claim, wherein said modulating means varies the strength of connection between adjacent amplifier stages.

7. A frequency divider circuit according to claim 5,

wherein said modulating means varies the hysteresis of each of said amplifier stages.

8. A frequency divider circuit according to any preceding claim, wherein said frequency divider circuit is a FET type semiconductor circuit.

9. A frequency divider circuit according to claim 8, integrated monolithically with complementary FET logic.

10. A frequency divider circuit according to claim 8, wherein said frequency divider circuit is a CMOS circuit integrated monolithically with CMOS logic circuitry in a standard CMOS process.

11. A frequency divider circuit according to any preceding claim, suitable for use where the frequency of the input signal to be divided is greater than 100 MHz.

12. A frequency divider circuit according to any preceding claim, further comprising logic means for providing dividing by ratios other than simple powers of two.

13. A frequency divider circuit according to any preceding claim, wherein each of said amplifier stages comprises a latch circuit having two inverters connected in a memory arrangement with the output of one connected to the input of the other.

14. A semiconductor latch comprising:
a data input;
a data output;
a clock input;
two inverters connected in a memory arrangement with

the output of one connected to the input of the other; and

input means connected to said memory arrangement, for writing new data applied to said data input into said memory arrangement, in dependence upon a clock signal applied to said clock input;

characterised in that

said latch comprises varying means for varying the time taken for new data to be written into said memory arrangement.

15. A semiconductor latch according to claim 14, wherein said varying means varies the strength of connection between said input means and said memory arrangement.

16. A semiconductor latch according to claim 14, wherein said varying means varies the hysteresis of the memory arrangement.

17. A semiconductor latch according to claim 14, 15 or 16, wherein said latch is a FET type latch in an integrated circuit.

18. A semiconductor latch according to claim 17, wherein said latch is a CMOS latch in an integrated circuit.

19. A semiconductor latch according to any of claims 13 to 18, wherein said varying means varies the time taken for new data to be written into said memory arrangement in response to a clock signal applied to said clock input.

20. A method of frequency division using an even number of amplifier stages connected in series with the output of the last amplifier stage connected to the input of the

first amplifier stage, the method comprising:

modulating the propagation delay through each of said amplifier stages, about the period of the input signal to be divided, such that when the propagation delay through odd-numbered amplifier stage(s) increases, the propagation delay through even-numbered amplifier stage(s) decreases.

21. A method according to claim 20, wherein each amplifier is a differential amplifier.

22. A method according to claim 20 or 21, wherein each amplifier stage used comprises an amplifier with hysteresis.

23. A method according to claim 20, 21 or 22, wherein said modulating step varies the strength of connection between adjacent amplifier stages.

24. A method according to claim 22, wherein said modulating step varies the hysteresis of each of said amplifier stages.

25. A method according to any of claims 20 to 24, wherein said amplifier stages comprise an FET type semiconductor integrated circuit.

26. A method according to claim 25, wherein said amplifier stages comprise a CMOS integrated circuit.

27. A method according to any of claims 20 to 26, wherein the frequency of the input signal to be divided is greater than 100 MHz.

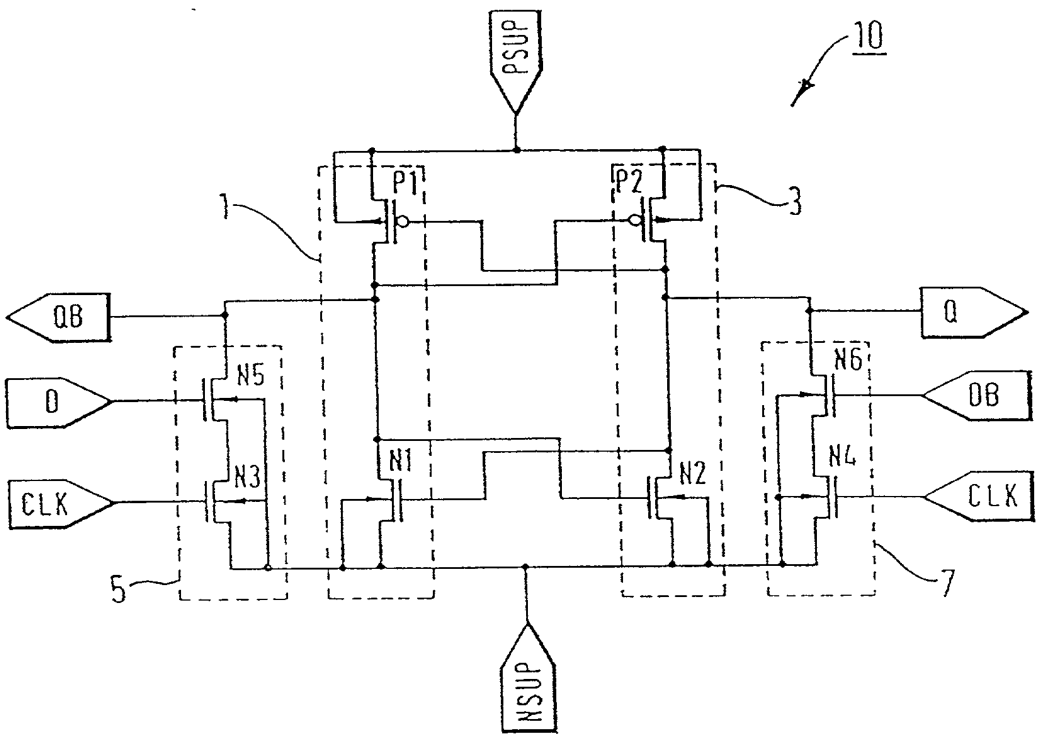
28. A method according to any of claims 20-27, wherein

said method also uses logic circuits for providing division by ratios other than simple powers of two.

29. A radio receiver comprising a frequency divider circuit according to any of claims 1 to 12 or utilising a method of frequency division according to any of claims 20 to 28.

30. A radio receiver comprising a latch circuit according to any of claims 13 to 19.

FIG. 1a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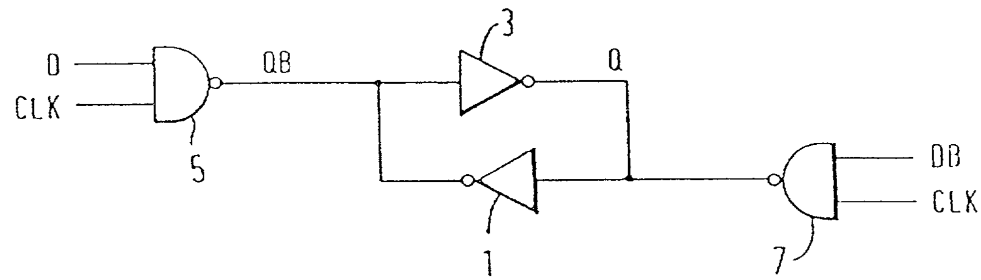
10
1
P1
P2
3
QB
Q
D
N5
N6
DB
CLK
N3
N1
N2
N4
CLK
5
7
NSUP

FIG. 1b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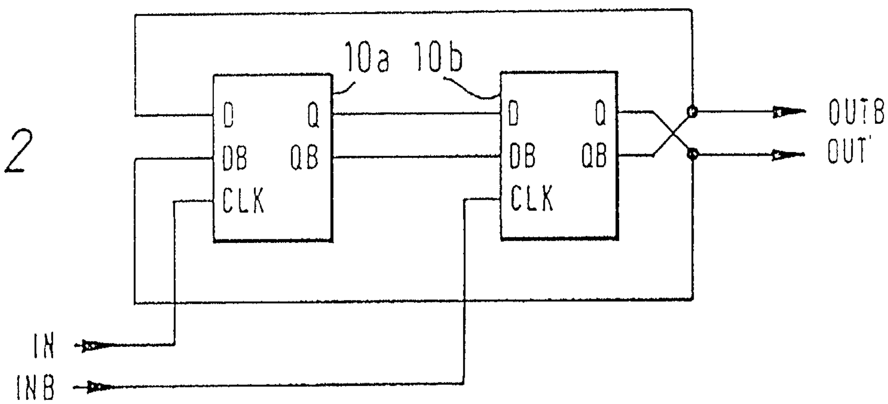
5
1
DB
CLK
7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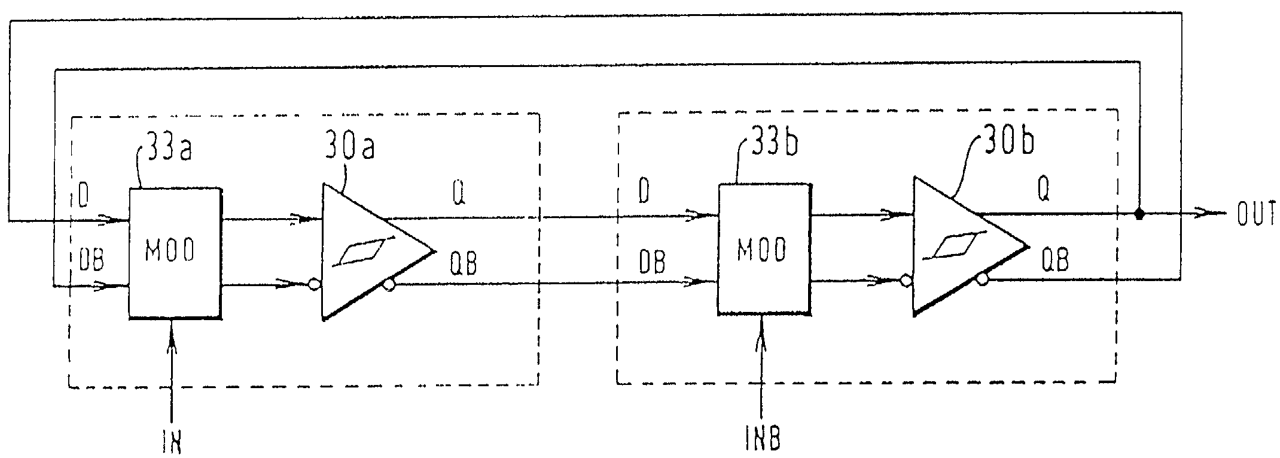
QB
OUTB
OUT
IN
INB

FIG. 2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MOD
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QB
OUT
IN
INB

FIG. 3

FIG. 4

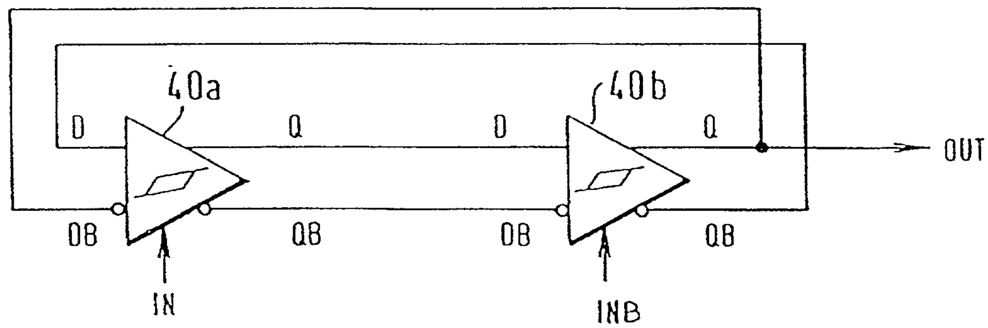


FIG. 5

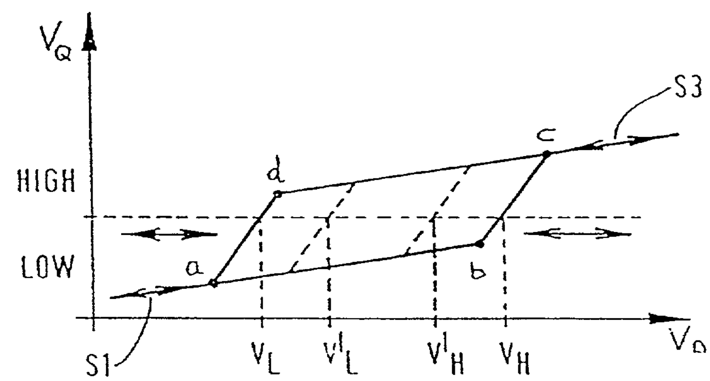
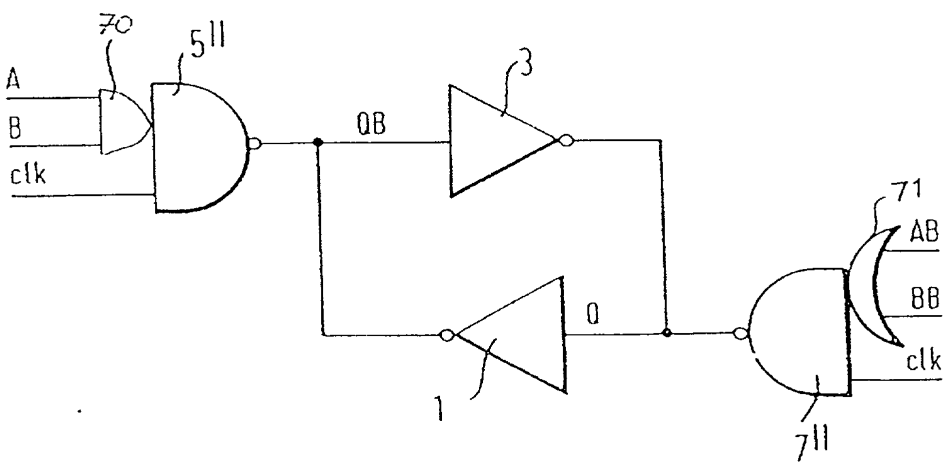


FIG. 7b



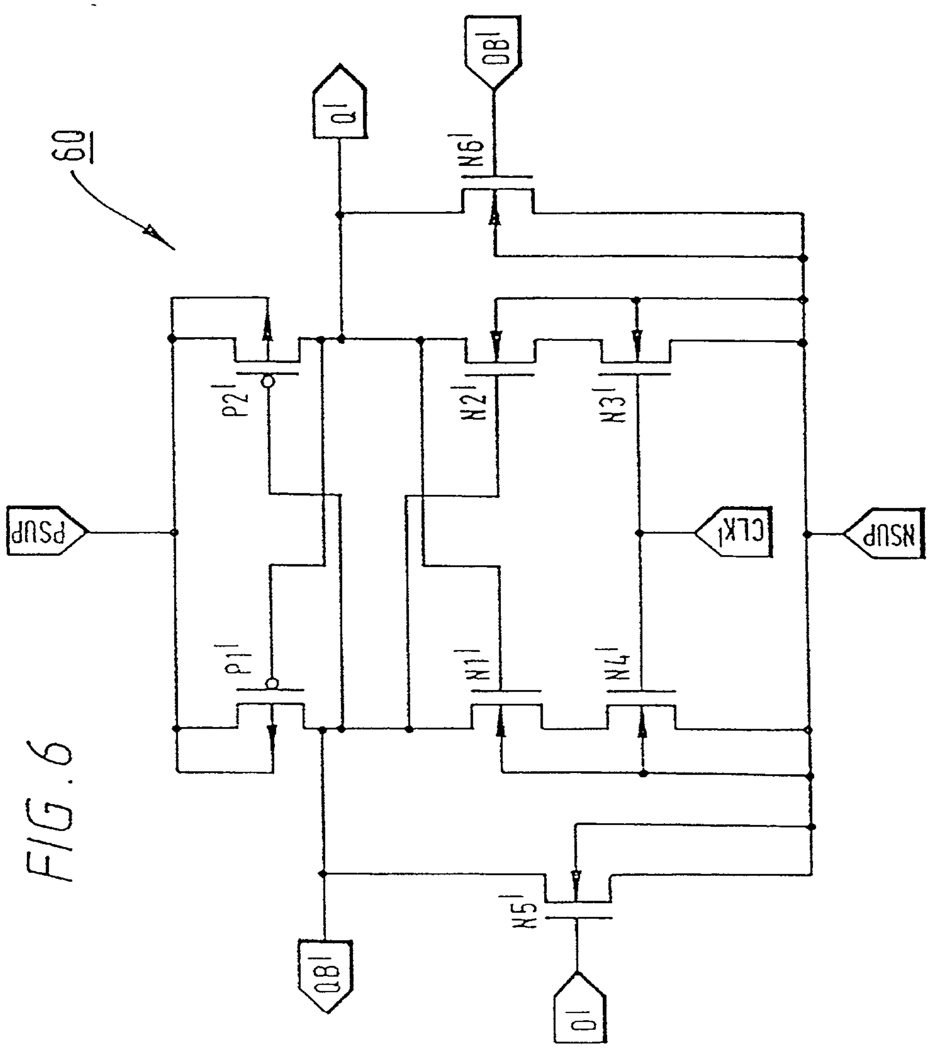
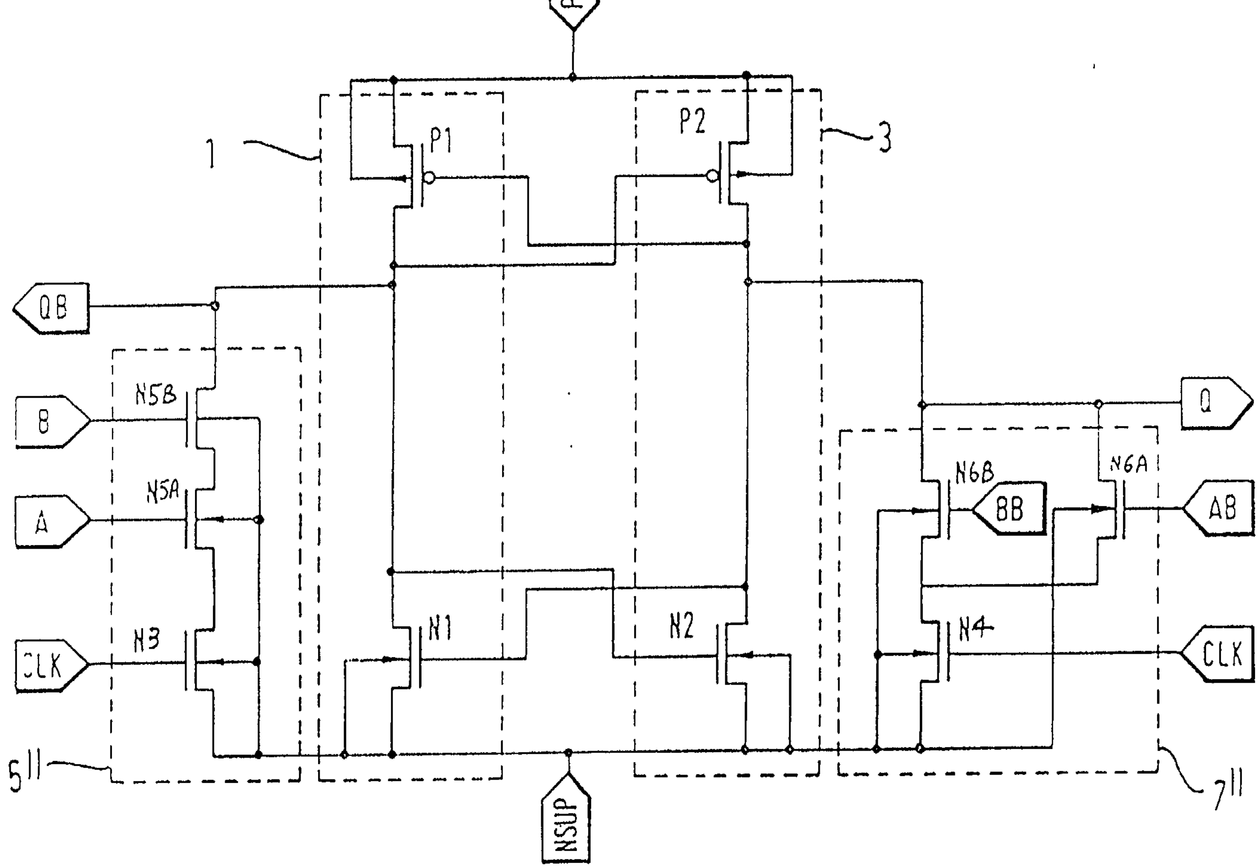


FIG. 6

FIG. 7a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P2
1
3
QB
B
A
CLK
N5B
N5A
N3
N1
N2
Q
N6B
BB
N6A
AB
N4
CLK
5
7
NSUP

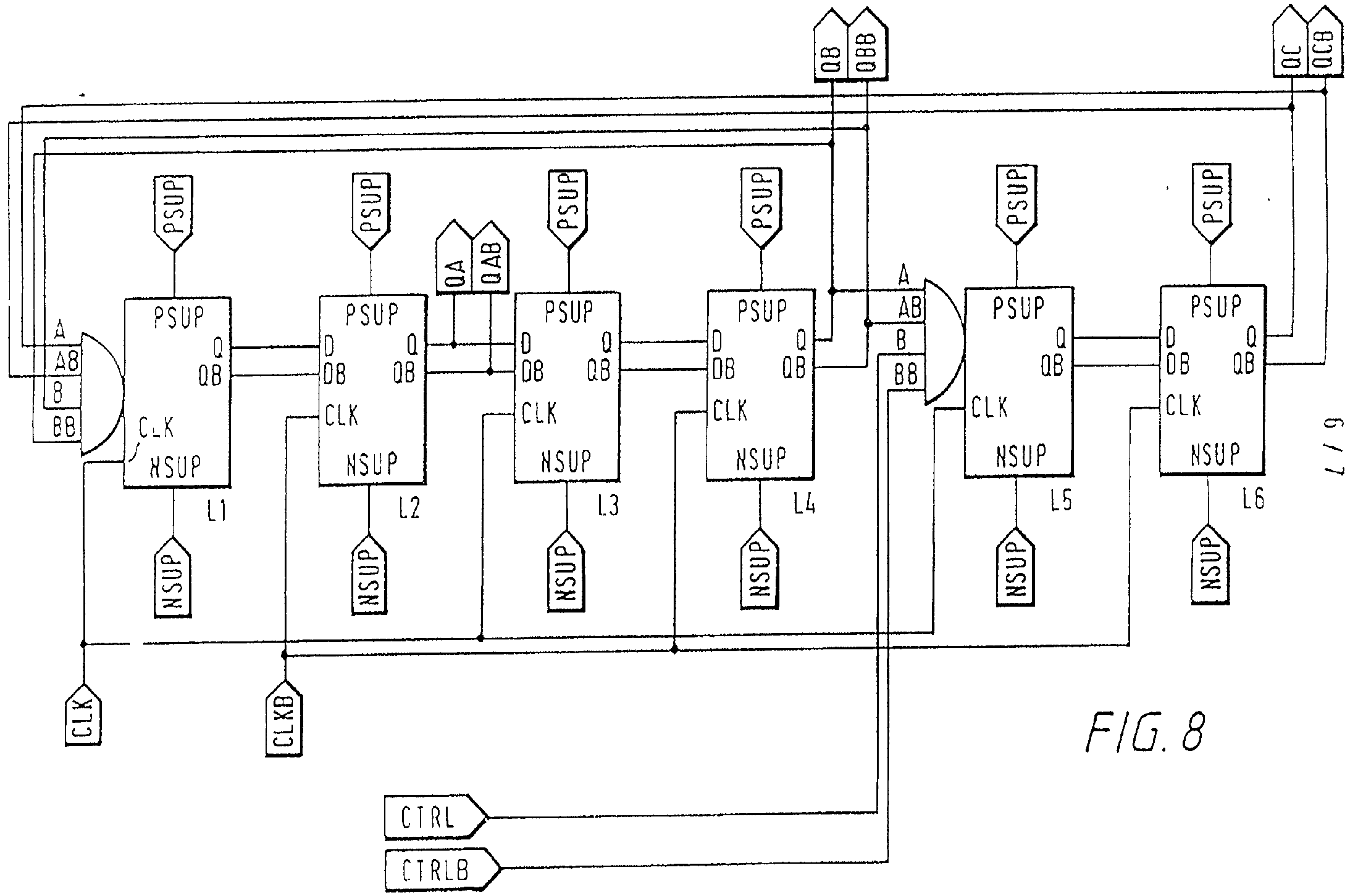
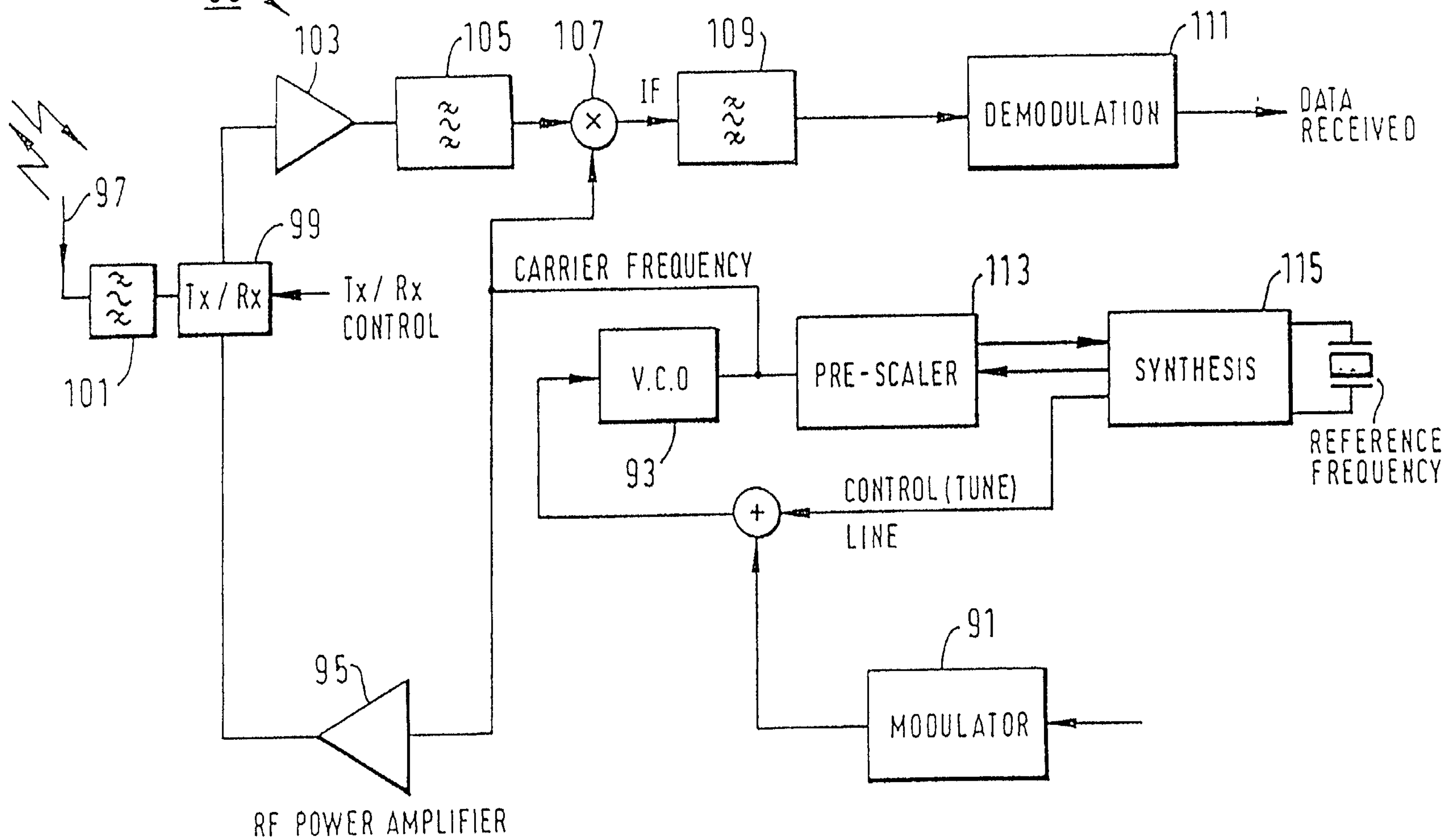

PSUP
NSUP
D
DB
Q
QB
CLK
A
AB
B
BB
L1
L2
L3
L4
L5
L6
QA
QAB
QB
QBB
QC
QCB
CLK
CLKB
CTRL
CTRLB

FIG. 8

FIG. 9


90
103
105
107
109
111
IF
DEMODULATION
DATA RECEIVED
97
99
101
Tx / Rx
Tx / Rx CONTROL
CARRIER FREQUENCY
113
115
V.C.O
PRE-SCALER
SYNTHESIS
REFERENCE FREQUENCY
93
CONTROL (TUNE) LINE
91
95
MODULATOR
RF POWER AMPLIFIER

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

United States Patent Application

COMBINED DECLARATION AND POWER OF ATTORNEY

As a below named inventor I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that

I verily believe I am the original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled: **INTEGRATED CIRCUIT**.

The specification of which is attached hereto.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with 37 C.F.R. § 1.56 (attached hereto). I also acknowledge my duty to disclose all information known to be material to patentability which became available between a filing date of a prior application and the national or PCT international filing date in the event this is a Continuation-In-Part application in accordance with 37 C.F.R. §1.63(e).

I hereby claim foreign priority benefits under 35 U.S.C. §119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on the basis of which priority is claimed:

Foreign application(s), if any, claiming priority under 35 U.S.C. § 119:

Application Number	Country	Day/Month/Year Filed
9721082.7	**Great Britain**	**03/10/1997**

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

No such claim for priority is being made at this time.

I hereby claim the benefit under 35 U.S.C. § 120 or 365(c) of any United States and PCT international application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose material information as defined in 37 C.F.R. § 1.56(a) which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status
PCT/GB98/02963	**October 2, 1998**	**Pending**

I hereby appoint the following attorney(s) and/or patent agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith:

Anglin, J. Michael	Reg. No. 24,916	Jurkovich, Patti J.	Reg. No. 44,813	Nelson, Albin J.	Reg. No 28,650
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Billion, Richard E.	Reg. No. 32,836	Kaufmann, John D.	Reg. No. 24,017	Oh, Allen J.	Reg. No. 42,047
Black, David W.	Reg. No. 42,331	Klima-Silberg, Catherine I.	Reg. No. 40,052	Padys, Danny J.	Reg. No. 35,635
Brennan, Leoniede M.	Reg. No. 35,832	Kluth, Daniel J.	Reg. No. 32,146	Parker, J. Kevin	Reg. No. 33,024
Brennan, Thomas F.	Reg. No. 35,075	Lacy, Rodney L.	Reg. No. 41,136	Perdok, Monique M.	Reg. No. 42,989
Brooks, Edward J., III	Reg. No 40,925	Leffert, Thomas W	Reg. No. 40,697	Prout, William F.	Reg. No. 33,995
Chu, Dinh C.P.	Reg. No 41,676	Lemaire, Charles A.	Reg. No. 36,198	Schumm, Sherry W.	Reg. No. 39,422
Clark, Barbara J.	Reg. No. 38,107	Litman, Mark A.	Reg. No. 26,390	Schwegman, Micheal L.	Reg. No. 25,816
Dahl, John M.	Reg. No. 44,639	Lundberg, Steven W.	Reg. No 30,568	Smith, Michael G.	Reg. No. 45,368
Drake, Eduardo E.	Reg. No. 40,594	Mack, Lisa K.	Reg. No. 42,825	Speier, Gary J.	Reg. No. 45,458
Eliseeva, Maria M.	Reg. No. 43,328	Maeyaert, Paul L.	Reg. No. 40,076	Steffey, Charles E.	Reg. No. 25,179
Embretson, Janet E.	Reg. No. 39,665	Maki, Peter C.	Reg. No. 42,832	Terry, Kathleen R.	Reg. No. 31,884
Fordenbacher, Paul J.	Reg. No. 42,546	Malen, Peter L.	Reg. No. 44,894	Tong, Viet V.	Reg. No. 45,416
Forrest, Bradley A.	Reg. No. 30,837	Mates, Robert E.	Reg. No. 35,271	Viksnins, Ann S.	Reg. No. 37,748
Harris, Robert J.	Reg. No. 37,346	McCrackin, Ann M.	Reg. No. 42,858	Woessner, Warren D.	Reg. No. 30,440
Huebsch, Joseph C.	Reg. No. 42,673	Nama, Kash	Reg. No. 44,255		

I hereby authorize them to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/organization/who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct Schwegman, Lundberg, Woessner & Kluth, P.A. to the contrary.

Please direct all correspondence in this case to **Schwegman, Lundberg, Woessner & Kluth, P.A.** at the address indicated below:

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Telephone No. (612)373-6900

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Signature: ______________________ Date: ______________________
Ian Michael Sabberton

§ 1.56 Duty to disclose information material to patentability.

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclose information exists with respect to each pending claim until the claim is canceled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is canceled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclose all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§ 1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) the closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made of record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application:

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.